This listing of claims will replace all prior versions, and listings, of claims in the application:

## Claim 1 (canceled)

- 1 Claim 2 (currently amended): An apparatus for processing a
- 2 block of data representing at least one symbol, the
- 3 apparatus comprising:
- 4 a jitter compensation filter for performing a
- 5 filtering operation on said block of data to generate a
- 6 filtered block of data, the jitter compensation filter
- 7 having an update input for receiving a filter coefficient
- 8 update signal;
- an error calculation module coupled to the update
- 10 input of the jitter compensation filter, the error
- 11 compensation module generating the filter coefficient
- 12 update signal from at least one signal error estimate made
- 13 from the filtered block of data output by the jitter
- 14 compensation filter; and
- 15 The apparatus of claim 1, further comprising:
- 16 a control circuit coupled to said error
- 17 calculation circuit module for determining as a function of
- 18 said at least one signal error estimate, when to output
- 19 said filtered block of data.
  - 1 Claim 3 (currently amended): The apparatus of claim  $\frac{1}{2}$ ,
- 2 further comprising:
- a channel compensation circuit for receiving said
- 4 block of data and performing a channel compensation
- 5 operation on at least a portion of said block of data prior
- 6 to the block of data being processed by said jitter
- 7 compensation filter.

| 1  | Claim 4 (original): The apparatus of claim 3, wherein said          |
|----|---|
| 2  | block of data represents a plurality of symbols, the                |
| 3  | apparatus further comprising:                                       |
| 4  | demodulator circuitry coupled to an output of the                   |
| 5  | jitter compensation filter.   |
|    |   |
| 1  | Claim 5 (currently amended): The apparatus of claim $\frac{1}{2}$ , |
| 2  | where wherein the error calculation module includes:                |
| 3  | means for generating a decision directed error                      |
| 4  | value.  |
|    |   |
| 1  | Claim 6 (currently amended): The apparatus of claim 5,              |
| 2  | wherein the error calculation module further includes:              |
| 3  | An apparatus for processing a block of data representing at         |
| 4  | least one symbol, the apparatus comprising:                         |
| 5  | a jitter compensation filter for performing a                       |
| 6  | filtering operation on said block of data to generate a             |
| 7  | filtered block of data, the jitter compensation filter              |
| 8  | having an update input for receiving a filter coefficient           |
| 9  | update signal; and  |
| 10 | an error calculation module coupled to the update                   |
| 11 | input of the jitter compensation filter, the error                  |
| 12 | compensation module generating the filter coefficient               |
| 13 | update signal from at least one signal error estimate made          |
| 14 | from the filtered block of data output by the jitter                |
| 15 | compensation filter, wherein the error calculation module           |
| 16 | includes:   |
| 17 | means for generating a decision                                     |
| 18 | directed error value;   |
| 19 | means for generating a pilot  |
| 20 | directed error value; and   |

| 21 | a selection device for selecting                            |
|----|---|
| 22 | one of the decision directed error value and the            |
| 23 | pilot directed error value to be output.                    |
|    |   |
| 1  | Claim 7 (currently amended): The apparatus of claim 5,      |
| 2  | wherein said error estimation module further includes:      |
| 3  | An apparatus for processing a block of data representing at |
| 4  | least one symbol, the apparatus comprising:                 |
| 5  | a jitter compensation filter for performing a               |
| 6  | filtering operation on said block of data to generate a     |
| 7  | filtered block of data, the jitter compensation filter      |
| 8  | having an update input for receiving a filter coefficient   |
| 9  | update signal; and  |
| 10 | an error calculation module-coupled to the update           |
| 11 | input of the jitter compensation filter, the error          |
| 12 | compensation module generating the filter coefficient       |
| 13 | update signal from at least one signal error estimate made  |
| 14 | from the filtered block of data output by the jitter        |
| 15 | compensation filter, wherein the error calculation module   |
| 16 | includes:   |
| 17 | means for generating a decision directed                    |
| 18 | error_value;  |
| 19 | means for generating a non-decision directed                |
| 20 | error value; and  |
| 21 | a selection device for selecting one of the                 |
| 22 | decision directed error value and the non-                  |
| 23 | decision directed error value to be output.                 |
| •  |   |
| 1  | Claim 8 (currently amended): The apparatus of claim 7,      |
| 2  | further comprising:   |
| 3  | an input buffer coupled to the jitter                       |
| 4  | compensation filter for storing said block of data while it |

- 5 is being processed multiple times by said jitter
- 6 compensation filter.

## Claims 9 and 10 (canceled)

- 1 Claim 11 (currently amended): The apparatus of claim 10,
- 2 further comprising:
- 3 An apparatus for processing a block of data representing at
- 4 least one symbol, the apparatus comprising:
- a jitter compensation filter for performing a
- 6 filtering operation on said block of data to generate a
- 7 filtered block of data, the jitter compensation filter
- 8 having an update input for receiving a filter coefficient
- 9 update signal;
- 10 an error calculation module coupled to the update
- 11 input of the jitter compensation filter, the error
- 12 compensation module generating the filter coefficient
- 13 update signal from at least one signal error estimate made
- 14 from the filtered block of data output by the jitter
- 15 compensation filter;
- .16 an input buffer for storing said block of <u>data</u>
- 17 while being processed multiple times by said jitter
- 18 compensation filter; and
- an output control device for determining when to
- 20 output the filtered block of data generated by said jitter
- 21 compensation filter.
  - 1 Claim 12 (original): The apparatus of claim 11, wherein
  - 2 the output control device includes:
  - 3 means for determining when said block of data has
  - 4 been filtered a fixed number of times by the jitter
  - 5 compensation filter.

- 1 Claim 13 (original): The apparatus of claim 11,
- wherein the output control device includes an
- 3 input for receiving the filter coefficient update signal
- 4 generated by said error calculation module; and
- 5 wherein the jitter compensation filter further
- 6 includes means for resetting filter coefficient values to a
- 7 set of initial values in response to a reset signal
- 8 generated by said output control device.
- 1 Claims 14 and 15 (canceled)
- 1 Claim 16 (currently amended): The system of claim 15,
- 2 further comprising;
- 3 A system for processing a multi-tone signal, the system
- 4 including:
- a channel compensation module for performing a
- 6 channel compensation operation on said multi-tone signal;
- 7 a jitter compensation module coupled to an output
- 8 of the channel compensation module for performing a jitter
- 9 reduction operation on the channel compensated multi-tone
- 10 signal, wherein the jitter compensation module includes : a
- 11 jitter compensation filter with programmable filter tap
- 12 weights, and means for iteratively updating the filter tap
- 13 weights as a function of the jitter compensation filter
- 14 output; and
- 15 a control circuit for determining when the output
- 16 of the jitter compensation filter should be used as the
- 17 output of the jitter compensation module.

- 1 Claim 17 (currently amended): The system of claim 15 16,
- wherein the means for iteratively updating the filter tap
- 3 weights includes:
- a signal error estimation circuit for generating
- 5 from the output of the jitter compensation filter a measure
- 6 of a symbol error.
- 1 Claim 18 (currently amended): The system of claim 17,
- 2 further comprising:
- 3 A system for processing a multi-tone signal, the system
- 4 including:
- a channel compensation module for performing a
- 6 channel compensation operation on said multi-tone signal;
- 7 a jitter compensation module coupled to an output
- 8 of the channel compensation module for performing a jitter
- 9 reduction operation on the channel compensated multi-tone
- 10 signal, wherein the jitter compensation module includes : a
- 11 jitter compensation filter with programmable filter tap
- 12 weights, and means for iteratively updating the filter tap
- 13 weights as a function of the jitter compensation filter
- 14 output, wherein the means for iteratively updating the
- 15 filter tap weights includes a signal error estimation
- 16 circuit for generating from the output of the jitter
- 17 compensation filter a measure of a symbol error; and
- means for resetting the jitter compensation
- 19 filter tap weights to an initial set of values in response
- 20 to the control circuit determining that the output of the
- 21 jitter compensation filter should be used as the output of
- 22 the jitter compensation filter.
- 1 Claim 19 (currently amended): A method of using a filter
- 2 having a plurality of tap weights to reduce the an effect.

- 3 of phase jitter on a block of data representing at least
- 4 one transmitted symbol, the method comprising the steps of:
- i) operating said filter to filter said block of
- 6 samples to produce a filtered block of data;
- 7 ii) determining a signal error from the filtered
- 8 block of data;
- 9 iii) updating at least one of said plurality of
- 10 tap weights in said filter as a function of the determined
- 11 signal error; and
- iv) repeating steps i, ii, and iii until a filter
- 13 updating stop criterion is satisfied.
  - 1 Claim 20 (original): The method of claim 19, further
- 2 comprising the step of:
- 3 supplying the filtered block of data output by
- 4 said filter when said filter updating criterion is
- 5 satisfied to subsequent receiver circuitry.
- 1 Claim 21 (original): The method of claim 19, wherein said
- 2 filter updating stop criterion is the completion of a fixed
- 3 number of filtering operations on said block of data.
- 1 Claim 22 (original): The method of claim 21, wherein said
- 2 filter updating criterion is a failure in the signal error
- 3 to exhibit an improvement over the previous signal error.
- 1 Claim 23 (original): The method of claim 19, wherein said
- 2 step of determining a signal error includes generating a
- 3 decision directed error value.

- 1 Claim 24 (original): The method of claim 19, wherein said
- 2 step of determining a signal error includes generating a
- 3 non-decision directed error value.
- 1 Claim 25 (original): The method of claim 19, further
- 2 comprising:
- 3 prior to performing step i, performing a channel
- 4 compensation operation on said block of data.
- 1 Claim 26 (original): The method of claim 25, a single
- 2 channel compensation operation is performed on the block of
- 3 data in a first period of time; and
- 4 step i, ii and iii are performed multiple times
- 5 in a time period which is equal to or shorter than the
- 6 first time period.